CLAIMS

What is claimed is:

1. A virtually parallel multiplier-accumulator (VMAC) responsive to a VMAC clock (VMCK) derived from a master clock (MCK), said VMAC being adapted for performing less than one multiplier-accumulator (MAC) operation within a MCK cycle, said VMAC comprising:

a control-wave generator (CWG) adapted for generating a plurality of control signals within a VMCK cycle; and

a sequential-computational stage MAC (SCS-MAC) adapted for receiving data from a source register and for receiving said plurality of control signals from said CWG, said SCS-MAC performing an operation on said data upon receipt of each of said plurality of control signals from said CWG.

2. A VMAC as recited by claim 1, wherein said SCS-MAC comprises:

a partial product generator (PPG) adapted for receiving a first data and a second data from a source register and for generating an output that is a product of said first and said second data; and

a multi-stage partial product adder (PPA) adapted for receiving said PPG output and for receiving a third data, said PPA generating an output that is the sum of said PPG output and said third data.

3. A VMAC as recited by claim 2, wherein said PPA further comprises a plurality of serially arranged stages that define a data path through said PPA.

4. A VMAC as recited by claim 3, wherein each of said plurality of serially arranged stages receives an input from an immediately preceding stage and generates an output that is a partial sum of said input.

5. A VMAC as recited by claim 1, wherein each of said serially arranged stages defines a worst-case delay period, and wherein said CWG further comprises a delay data path that includes a plurality of delay stages, each of said plurality of delay stages defining a delay that is substantially the same as the delay of a corresponding serially arranged stage.

6. A VMAC as recited by claim 1, wherein said VMAC is adapted for performing the same number of MAC operations within each MCK cycle.

7. A VMAC as recited by claim 1, wherein said VMAC is adapted for performing a different number of MAC operations within each MCK cycle.

8. A VMAC as recited by claim 3, wherein said PPA comprises a dynamic carry save adder stage and a dynamic carry look ahead stage.

9. A VMAC as recited by claim 2, wherein said PPA further comprises a plurality of serially arranged stages, said PPG and each of said serially arranged stages separately performing an operation on said data, wherein flow of said data through said PPG and each of said serially arranged stages of said PPA is controlled by a control signal generated by said CWG.

10. An integrated circuit including a virtually parallel multiplier-accumulator (VMAC) responsive to a VMAC clock (VMCK) derived from a master clock (MCK), said VMAC being adapted for performing less than one multiplier-accumulator (MAC) operation within a MCK cycle, said integrated circuit comprising:

a source register for providing data to said VMAC; and

a result register for receiving data from said VMAC and for providing data to said source register;

wherein said source register provides parallel data to said VMAC and wherein said VMAC provides serial data output, said integrated circuit further comprising an output data demultiplexer and a register for receiving said serial data output from said VMAC, for converting said serial data to parallel data, and for communicating said parallel data to said result register.

11. An integrated circuit as recited by claim 10, wherein said integrated circuit comprises a microprocessor.

12. An integrated circuit as recited by claim 10, wherein said integrated circuit comprises a digital signal processor.

13. An integrated circuit as recited by claim 10, wherein said VMAC is adapted for performing the same number of MAC operations within each MCK cycle.

14. An integrated circuit as recited by claim 10, wherein said VMAC is adapted for performing a different number of MAC operations within each MCK cycle.

15. An integrated circuit as recited by claim 11, wherein said VMAC comprises:

a control-wave generator (CWG) adapted for generating a plurality of control signals within a VMCK cycle; and

a sequential-computational stage MAC (SCS-MAC) adapted for receiving data from a source register and for receiving said plurality of control signals from said CWG, said SCS-MAC performing an operation on said data upon receipt of each of said plurality of control signals from said CWG.

16. An integrated circuit as recited by claim 15, wherein said SCS-MAC comprises:

a partial product generator (PPG) adapted for receiving a first data and a second data from a source register and for generating an output that is a product of said first and said second data; and

a multi-stage partial product adder (PPA) adapted for receiving said PPG output and for receiving a third data, said PPA generating an output that is the sum of said PPG output and said third data.

17. An integrated circuit as recited by claim 16, wherein said PPA further comprises a plurality of serially arranged stages, said PPG and each of said serially arranged stages separately performing an operation on said data, wherein flow of said data through said PPG and each of

said serially arranged stages of said PPA is controlled by a control signal generated by said CWG.